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EXAMINER	
MATISIAK, JENNIFER E	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/814,816	ZHANG ET AL.	
	Examiner	Art Unit	
	Jennifer Matisiak	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-63 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-16,18-21,26-34,36-57 and 59-63 is/are rejected.

7)☒ Claim(s) 17,22-25, 28, 35 and 58 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 31 March 2004 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 05032004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claim 40 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding claim 40, the applicant does not mention the manner in which a computer-readable medium performs the function of encoding.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 40 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant does not clarify whether the integrated circuit product or the computer-readable medium comprises the inductor and enclosure.

3. Claims 37-38 recite the limitation " the electromagnetic shielding structure." There is insufficient antecedent basis for this limitation in the claim.

4. Claim 62 recites the limitation " the apparatus." There is insufficient antecedent basis for this limitation in the claim.

Specification

5. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Regarding claim 28, applicant does not disclose "an amplifier circuit coupled in parallel with the inductor structure."

Drawings

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 1000, 1002, 1004, 1006, 1008, 1010, 1016 and 1066. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and

informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3, 6-8, 13-16 18, 21, 26, 29-31, 36-39, 41-44, 47, 52, 56-57, 59 and 61-63 rejected under 35 U.S.C. 102(b) as being anticipated by Liou et al. (US 6037649), hereinafter Liou.

Regarding claim 1, Liou discloses an apparatus (Fig. 3C, for example) comprising: an electromagnetic shielding structure (S3 33, S2 32, S1 31, 27, 24) formed at least partially in one or more redistribution layers (see figure below) formed on an integrated circuit die (col 4, lines 57-60), the electromagnetic shielding structure substantially surrounding a circuit element (M3 28, M2 25, M1 22, 27, 24).

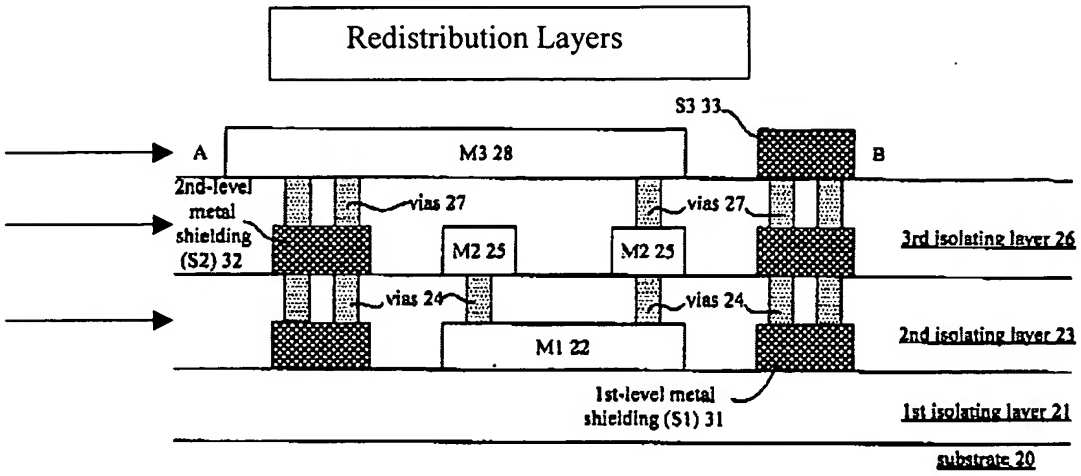

FIG. 3B

Regarding claim 2, Liou discloses an apparatus (Fig. 3C) wherein the circuit element is formed at least partially in the one or more redistribution layers (see figure above).

Regarding claim 3, Liou discloses an apparatus (Fig. 3C) wherein the redistribution layers (see figure above) are formed above a passivation layer (23) of the integrated circuit die (col 4, lines 57-60).

Regarding claim 6, Liou discloses an apparatus (Fig. 3C) wherein the electromagnetic shielding structure (S3 33, S2 32, S1 31, 27, 24) has a top plate (S3 33), a bottom plate (S1 31), and sidewalls (S2 32).

Regarding claim 7, Liou discloses an apparatus (Fig. 3C) wherein the circuit element (M3 28, M2 25, M1 22, 27, 24) is substantially equidistant between the top (S3 33) and bottom plates (S1 31).

Regarding claim 8, Liou discloses an apparatus (Fig. 3C) wherein the circuit element (M3 28, M2 25, M1 22, 27, 24) is positioned between the top (S3 33) and bottom (S1 31) plates. Liou does not explicitly recite "based at least in part on resistivities of the top and bottom plates." However this limitation is not given any patentable weight since it does not further limit the scope of the invention. It merely recites a consideration that went into the design process without specifically pointing out any characteristics.

Regarding claim 13, Liou discloses an apparatus (Fig. 3C) wherein the sidewalls (S2 32) of the electromagnetic shielding structure (S3 33, S2 32, S1 31, 27, 24) are formed at least in part by via structures (27, 24) in the integrated circuit die (col 4, lines 16-17).

Regarding claim 14, Liou discloses an apparatus (Fig. 3C) wherein the sidewalls (S2 32) of the electromagnetic shielding structure (S3 33, S2 32, S1 31, 27, 24) are formed at least in part by solid via structures (27, 24) in the redistribution layers (see figure above).

Regarding claim 15, Liou discloses an apparatus (Fig. 3C) wherein the sidewalls (S2 32) of the electromagnetic shielding structure (S3 33, S2 32, S1 31, 27, 24) are formed at least in part by discrete via structures (27, 24) in the redistribution layers (see figure above).

Regarding claim 16, Liou discloses an apparatus (Fig. 3C) wherein the discrete via structures (27, 24) in the redistribution layers are stacked (see figure above).

Regarding claim 18, Liou discloses an apparatus (Fig. 3C) wherein the redistribution layers (see figure above) include at least one redistribution metal layer (M3 28) and at least one redistribution dielectric layer (26).

Regarding claim 21, Liou discloses an apparatus (Fig. 3C) wherein the circuit element (M3 28, M2 25, M1 22, 27, 24) comprises an inductor structure (col 4, lines 53-54).

Regarding claim 26, Liou discloses an apparatus (Fig. 3C) wherein the inductor structure comprises a series-connected pair of inductor loops (Fig. 2A, for example).

Regarding claim 29, Liou discloses a method (Fig. 3C) comprising: electromagnetically shielding at least one circuit element (M3 28, M2 25, M1 22, 27, 24) formed on an integrated circuit die (col 4, lines 16-17) by substantially surrounding the circuit element with an electrically conductive enclosure (col 4, lines 57-60) formed at least partially in one or more redistribution layers (see figure above) formed on the integrated circuit die.

Regarding claim 30, Liou discloses a method (Fig. 3C) wherein the circuit element (M3 28, M2 25, M1 22, 27, 24) is formed at least partially in the redistribution layers (see figure above).

Regarding claim 31, Liou discloses a method (Fig. 3C) wherein the redistribution layers (see figure above) are formed above a passivation layer (23) of the integrated circuit die.

Regarding claim 36, Liou discloses a method (Fig. 3C) further comprising: providing the circuit element (M3 28, M2 25, M1 22, 27, 24) spaced from the electrically

conductive enclosure (S3 33, S2 32, S1 31, 27, 24) sufficiently spaced to limit the capability of the electrically conductive enclosure from generating an electromagnetic field that counteracts an electromagnetic field generated by the circuit element.

Regarding claim 37, Liou discloses a method (Fig. 3C) further comprising: effectively shielding with the electromagnetic shielding structure (S3 33, S2 32, S1 31, 27, 24) the circuit element (M3 28, M2 25, M1 22, 27, 24) from electromagnetic signals. Liou does note explicitly recite "of particular frequencies generated by external elements." However, it is inherent that particular frequencies can include those frequencies exclusive of the self-resonating frequency of the inductor. Furthermore, it is inherent that the shielding structure of the invention of Liou effectively shields the circuit element of the invention of Liou from electromagnetic signal generated by external elements.

Regarding claim 38, Liou recites a method (Fig. 3C). Liou does not explicitly recite "further comprising: effectively preventing electromagnetic signals of particular frequencies generated by the circuit element from effecting external elements using the electromagnetic shielding structure." However, it is inherent that particular frequencies can include the self-resonating frequency of the circuit element (M3 28, M2 25, M1 22, 27, 24). Furthermore, it is inherent that the shielding structure (S3 33, S2 32, S1 31, 27, 24) of the invention of Liou effectively prevents the circuit element of the invention of Liou from effecting external elements.

Regarding claim 39, Liou discloses a method (Fig. 3C) wherein the circuit element (M3 28, M2 25, M1 22, 27, 24) is an inductor structure.

Regarding claim 41, Liou discloses a method of manufacturing an integrated circuit product (Fig. 3C) comprising: forming an electromagnetic shielding structure (S3 33, S2 32, S1 31, 27, 24) at least partially in one or more redistribution layers (see figure above) formed on an integrated circuit die (col 4, lines 57-60), the electromagnetic shielding structure substantially surrounding a circuit element (M3 28, M2 25, M1 22, 27, 24).

Regarding claim 42, Liou discloses a method (Fig. 3C) further comprising: forming the circuit element (M3 28, M2 25, M1 22, 27, 24) at least partially in the redistribution layers (see figure above).

Regarding claim 43, Liou discloses a method (Fig. 3C) further comprising: forming a passivation layer (23).

Regarding claim 44, Liou discloses a method (Fig. 3C) further comprising: forming the redistribution layers (see figure above) above the passivation layer (23) of the integrated circuit die (col 4, lines 57-60).

Regarding claim 47, Liou discloses a method (Fig. 3C) wherein the electromagnetic shielding structure (S3 33, S2 32, S1 31, 27, 24) comprises an electrically conductive enclosure having a top plate (S3 33), a bottom plate (S1 31), and sidewalls (S2 32).

Regarding claim 52, Liou discloses a method (Fig. 3C) wherein the redistribution layers (see figure above) include at least one redistribution metal layer (M3 28) and at least one redistribution dielectric layer (26).

Regarding claim 56, Liou discloses a method (Fig. 3C) further comprising:

forming the sidewalls (S2 32) of the electromagnetic shielding structure (S3 33, S2 32, S1 31, 27, 24) at least in part with via structures (27, 24) in the redistribution layers (see figure above).

Regarding claim 57, Liou discloses a method (Fig. 3C) wherein the via structures (27, 24) are stacked in the redistribution layers (see figure above).

Regarding claim 59, Liou discloses a method (Fig. 3C) wherein the circuit element comprises an inductor structure (M3 28, M2 25, M1 22, 27, 24).

Regarding claim 61, Liou discloses an integrated circuit (col 4, lines 16-17) comprising: means for electrically coupling nodes (30 of Fig. 3C) of an integrated circuit; means for routing (27) as part of the integrated circuit die an electrical connection between a contact pad (29 of Fig. 3A, for example) on an integrated circuit die and a location of a package contact (col 3, lines 59-62); and means for electromagnetically shielding the coupling means with a structure (S3 33, S2 32, S1 31, 27, 24) formed at least partially by the means for routing.

Regarding claim 62, Liou discloses an apparatus (col 4, lines 16-17) further comprising: means for reducing an electromagnetic field in the shielding (col 4, lines 60-66). Although Liou does not explicitly recite "means that counteract an electromagnetic field generated by the coupling means," it is inherent that an electromagnetic field in the shielding is generated in response to an electromagnetic field generated by the coupling means.

Regarding claim 63, Liou discloses an integrated circuit (col 4, lines 16-17) comprising: an inductor (M3 28, M2 25, M1 22, 27, 24 of Fig. 3C) formed in

redistribution layers (see figure above); and means for shielding the inductor (S3 33, S2 32, S1 31, 27, 24) utilizing at least a first portion of a redistribution layer.

7. Claims 1, 4-5, 18, 20, 29, 32-34, 41, 45-46, 52-53 and 60 rejected under 35 U.S.C. 102(b) as being anticipated by Aoki et al. (US 6501169), hereinafter Aoki.

Regarding claim 1, Aoki discloses an apparatus (Fig. 9A, for example) comprising: an electromagnetic shielding structure (19) formed at least partially in one or more redistribution layers (17, 19, 45) formed on an integrated circuit die (11, col 4, lines 15-18), the electromagnetic shielding structure substantially surrounding a circuit element (col 12, lines 62-66).

Regarding claim 4, Aoki discloses an apparatus (Fig. 9A) wherein the redistribution layers (17, 19, 45) are formed above integrated circuit pads (13).

Regarding claim 5, Aoki discloses an apparatus (Fig. 9A) wherein the circuit element (col 12, lines 62-66) is formed below a passivation layer (15) of the integrated circuit die (11, col 4, lines 15-18).

Regarding claim 18, Aoki discloses an apparatus (Fig. 9A) wherein the redistribution layers (17, 19, 45) include at least one redistribution metal layer (17) and at least one redistribution dielectric layer (45).

Regarding claim 29, Aoki discloses a method (Figs. 10A-10F, for example) comprising: electromagnetically shielding at least one circuit element (col 12, lines 62-66) formed on an integrated circuit die (11 of Fig. 9A, col 4, lines 15-18) by substantially surrounding the circuit element with an electrically conductive enclosure (19) formed at

least partially in one or more redistribution layers (17, 19, 45) formed on the integrated circuit die.

Regarding claim 32, Aoki discloses a method (Figs. 10A-10F) wherein the redistribution layers (17, 19, 45 of Fig. 9A) are formed above integrated circuit pads (13).

Regarding claim 33, Aoki discloses a method (Figs. 10A-10F) wherein the circuit elements (col 12, lines 62-66) formed below a passivation layer (15) of the integrated circuit die (11, col 4, lines 15-18).

Regarding claim 34, Aoki discloses a method (Figs. 10A-10F) further comprising: shielding (19 of Fig. 9A) using via structures (44) stacked in the redistribution layers (17, 19, 45).

Regarding claim 41, Aoki discloses a method of manufacturing an integrated circuit product (Figs. 10A-10F) comprising: forming an electromagnetic shielding structure (19 of Fig. 9A) at least partially in one or more redistribution layers (17, 19, 45) formed on an integrated circuit die (11 of Fig. 9A, col 4, lines 15-18), the electromagnetic shielding structure substantially surrounding a circuit element (col 12, lines 62-66).

Regarding claim 45, Aoki discloses a method (Figs. 10A-10F) further comprising: forming integrated circuit pads (13 of Fig. 9A); and forming the redistribution layers (17, 19, 45) above the integrated circuit pads.

Regarding claim 46, Aoki discloses a method (Figs. 10A-10F) wherein the circuit element (col 12, lines 62-66) is formed at least partially below a passivation layer (45 of Fig. 9A) of the integrated circuit die (11 of Fig. 9A, col 4, lines 15-18).

Regarding claim 52, Aoki discloses a method (Figs. 10A-10F) wherein the redistribution layers (17, 19, 45 of Fig. 9A) include at least one redistribution metal layer (17) and at least one redistribution dielectric layer (45).

Regarding claim 53, Aoki discloses a method (Figs. 10A-10F) wherein the redistribution metal layers (17, 19, 45 of Fig. 9A) include at least one of aluminum and copper (col 12, lines19-21).

Regarding claim 60, Aoki discloses a method (Figs. 10A-10F) wherein the circuit element (col 12, lines 62-66) comprises a capacitor structure (col 12, lines 62-66).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 9-12 and 48-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liou as applied respectively to claims 6 and 47 above, and further in view of Aoki.

Regarding claim 9, Liou discloses an apparatus (Fig. 3C) as recited in claim 6. Liou does not disclose "wherein at least one of the top plate or bottom plate of the electromagnetic shielding structure is formed in under bump metal." Aoki discloses an electromagnetic shielding structure (19 of Fig. 1B) formed in under bump metal (col 5, lines 41-48). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Liou by forming the top plate and bottom plate of the electromagnetic shielding structure in under bump metal since it is desirable to make the shielding layers more conductive since in this manner the shielding layers can further reduce electromagnetic interference.

Regarding claim 10, Liou discloses an apparatus (Fig. 3C) as recited in claim 6. Liou does not disclose "wherein the sidewalls of the electromagnetic shielding structure are formed at least in part by under bump metal." Aoki discloses an electromagnetic shielding structure (19 of Fig. 1B) formed by under bump metal (col 5, lines 41-48). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Liou by forming the sidewalls of the electromagnetic shielding structure by under bump metal since it is desirable to make the shielding layers more conductive since in this manner the shielding layers can further reduce electromagnetic interference.

Regarding claim 11, Liou discloses an apparatus (Fig. 3C) as recited in claim 6. Liou does not disclose "wherein the top plate and at least a portion of the sidewalls are formed by under bump metal." Aoki discloses an electromagnetic shielding structure (19 of Fig. 1B) formed by under bump metal (col 5, lines 41-48). It would have been

obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Liou by forming the top plate and at least a portion of the sidewalls of the electromagnetic shielding structure by under bump metal since it is desirable to make the shielding layers more conductive since in this manner the shielding layers can further reduce electromagnetic interference.

Regarding claim 12, Liou and Aoki disclose the limitations of claim 11 as shown above. Moreover, Liou discloses a top plate (S3 33) supported by via structures (27, 24) formed in the redistribution layers (see figure above).

Regarding claim 48, Liou discloses a method (Fig. 3C) as recited in claim 47. Liou does not disclose "further comprising: forming at least one of the top plate or bottom plate of the electrically conductive enclosure in under bump metal." Aoki discloses a method (Figs. 10A-10F) of forming an electromagnetic shielding structure (19 of Fig. 1B) in under bump metal (col 5, lines 41-48). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Liou by forming the top plate and bottom plate of the electromagnetic shielding structure in under bump metal since it is desirable to make the shielding layers more conductive since in this manner the shielding layers can further reduce electromagnetic interference.

Regarding claim 49, Liou discloses a method (Fig. 3C) as recited in claim 47. Liou does not discloses "further comprising: forming the sidewalls of the electromagnetic shielding structure at least in part in under bump metal." Aoki discloses a method (Figs. 10A-10F) of forming an electromagnetic shielding structure (19 of Fig.

1B) by under bump metal (col 5, lines 41-48). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Liou by forming the sidewalls of the electromagnetic shielding structure by under bump metal since it is desirable to make the shielding layers more conductive since in this manner the shielding layers can further reduce electromagnetic interference.

Regarding claim 50, Liou discloses a method (Fig. 3C) as recited in claim 47. Liou does not disclose "further comprising: forming the top plate and at least a portion of the sidewalls in under bump metal." Aoki discloses a method (Figs. 10A-10F) of forming an electromagnetic shielding structure (19 of Fig. 1B) by under bump metal (col 5, lines 41-48). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Liou by forming the top plate and at least a portion of the sidewalls of the electromagnetic shielding structure by under bump metal since it is desirable to make the shielding layers more conductive since in this manner the shielding layers can further reduce electromagnetic interference.

Regarding claim 51, Liou and Aoki disclose the limitations of claim 50. Furthermore, Liou discloses a method (Fig. 3C) further comprising: forming via structures (27, 24) in the redistribution layers (see figure above), the via structures supporting the top plate (S3 33).

9. Claims 19-20 and 54-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki.

Regarding claim 19, Aoki discloses an apparatus (Fig. 9A). Aoki does not explicitly recite "wherein the redistribution dielectric layer is at least 15 micrometer thick and a dielectric layer of the integrated circuit die is less than 1 micrometer thick." However:

"[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

Therefore it would have been obvious to one of ordinary skill in the art to arrive at the optimal value through routine experimentation since it is desirable to make the invention of Aoki electrically and structurally sound.

Regarding claim 20, Aoki discloses an apparatus (Fig. 9A). Aoki does not explicitly recite "wherein the redistribution dielectric layer is at least 15 micrometer thick." However, for the reasons disclosed above, it would have been obvious to one of ordinary skill in the art to arrive at the optimal value through routine experimentation since it is desirable to make the invention of Aoki electrically and structurally sound.

Regarding claim 54, Aoki discloses a method (Figs. 10A-10F). Aoki does not explicitly recite "wherein the redistribution dielectric layer is at least 5um thick and wherein a dielectric layer of the integrated circuit die is less than 11 micrometers thick." However, for the reasons disclosed above, it would have been obvious to one of ordinary skill in the art to arrive at the optimal value through routine experimentation since it is desirable to make the invention of Aoki electrically and structurally sound.

Regarding claim 55, Aoki discloses a method (Figs. 10A-10F). Aoki does not explicitly recite "wherein the redistribution dielectric layer is at least 15 um thick." However, for the reasons disclosed above, it would have been obvious to one of ordinary skill in the art to arrive at the optimal value through routine experimentation since it is desirable to make the invention of Aoki electrically and structurally sound.

10. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Liou as applied respectively to claim 21 above, and further in view of Onishi et al. (US 5456368), hereinafter Onishi.

Liou discloses the limitations of claim 21. Liou does not disclose "wherein the electromagnetic shielding structure (13) substantially surrounds at least one capacitor coupled in parallel with the inductor structure." Onishi discloses an apparatus (Fig. 5, for example) comprising: an electromagnetic shielding structure (12), an integrated circuit die (1), with the electromagnetic shielding structure substantially over one capacitor coupled in parallel with the inductor structure (19). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a capacitor coupled in parallel with the inductor structure (M1, M2, M3 of Fig. 3C) in the invention of Liou since it is desirable in radio frequency (RF) devices to make RF oscillators which are well known to comprise an inductor parallel-coupled to a capacitor.

Allowable Subject Matter

11. Claims 17, 22-25, 28, 35, 58 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer Matisiak whose telephone number is 571-272-2639. The examiner can normally be reached on Business Days 9:30a-6:30p EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 517-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DOUGLAS W. OWENS
PRIMARY EXAMINER

JEM